Test Report

Repeated Power Cycling Test Report for Renesas G2L A55 SOM

Rev1.0
2022-02-06

Version History

Version	Modification instructions	Author	Date
V1.0	Initial document.	yuge	2022-07-06

1. Test Objective

Objective: This test aims to evaluate the core board's performance under repeated power cycles and to check if there are any power-up failures.

Hardware Platform: WTB-G2LS_V02 industrial control board SBC launched by Weathink Technology (including the WTC-G2LS_V03 System-On-Module)

System Platform: Linux 5.10

2. Test Results

Based on the WTC-G2LS_V02 core board of the WTB-G2LS industrial control board (hereinafter referred to as the G2L industrial control board), the core board was subjected to repeated power cycling tests over 10,000 times. No power-up failures were observed.

The test passed.

3. Test Method

As shown in the diagram, a stable control machine was used to run the test software, which repeatedly powered the core board on and off while monitoring the debug serial port for a specified string of data. For instance, after the system boots into Linux, a series of messages are sent, indicating the completion of the boot process. If no message is received within a specified time (e.g., 30 seconds), it indicates a failure to boot.

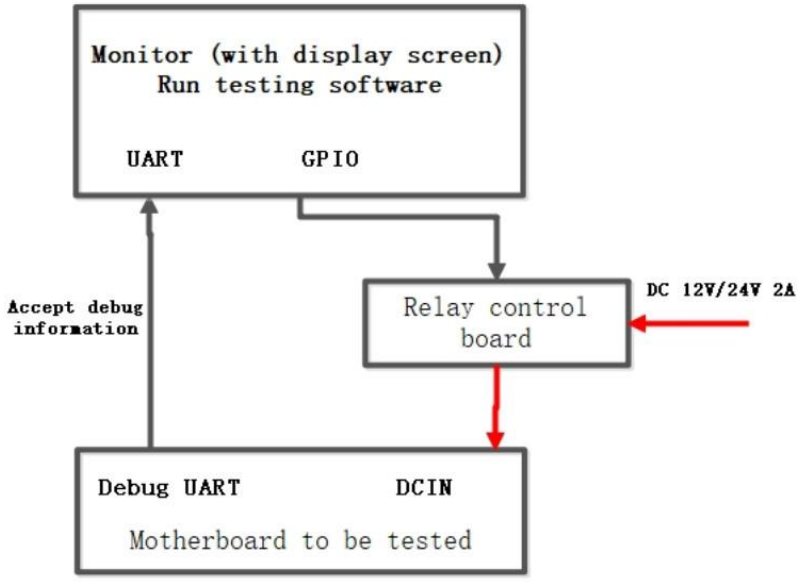

Figure 1: Diagram of Repeated Power Cycling Test

4. Test Process

A multi-channel oscilloscope was used to test the power signals on each channel of the core board.

Power IN	Count	Result
MotherBoard boot test (DC 12V IN)	10000+	PASS
MotherBoard boot test (DC 24V IN)	10000+	PASS

Figure 2: Test Results

Figure 3: Test Setup Image