RK3568S Core Board Datasheet

Rev. 1. 0
2022-09-01

Version Records

Version	Modified instructions	Modifier	Date
V1.0	Initial documentation	Zbb	2022-9-1

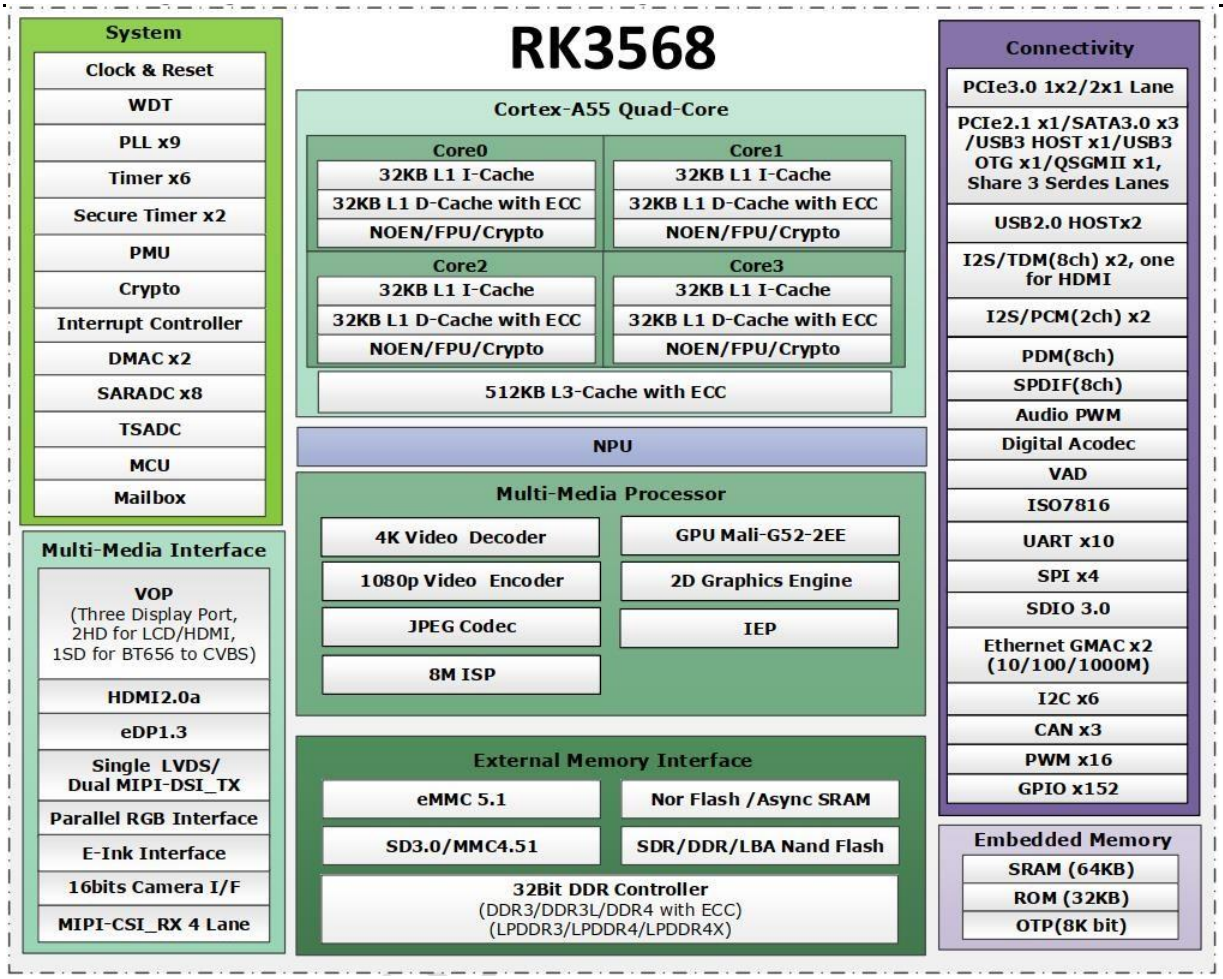
Catalog

Chapter 1 Product Introduction

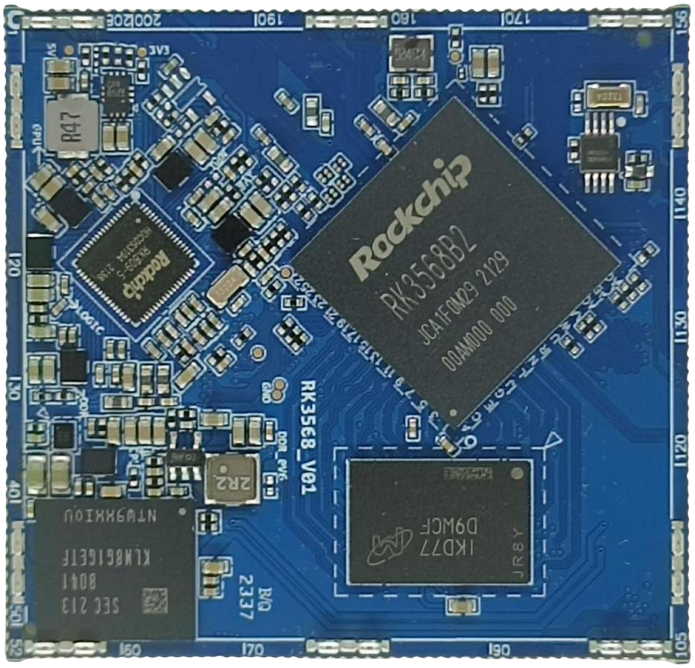
RK3568S core board is an embedded core board using Rockchip RK3568 series as the core MPU launched by our company. Based on ARM Cortex-A55 core, this series of devices has the characteristics of high performance, low power consumption, multi-interface and low cost. At the same time, it provides 3D graphics acceleration and integration of key peripherals, which can meet the needs of various applications. It supports mainstream DDR4 memory, and provides dual-channel Gigabit Ethernet and multi-channel serial port to meet the needs of industrial products.

1.1 CPU Performance

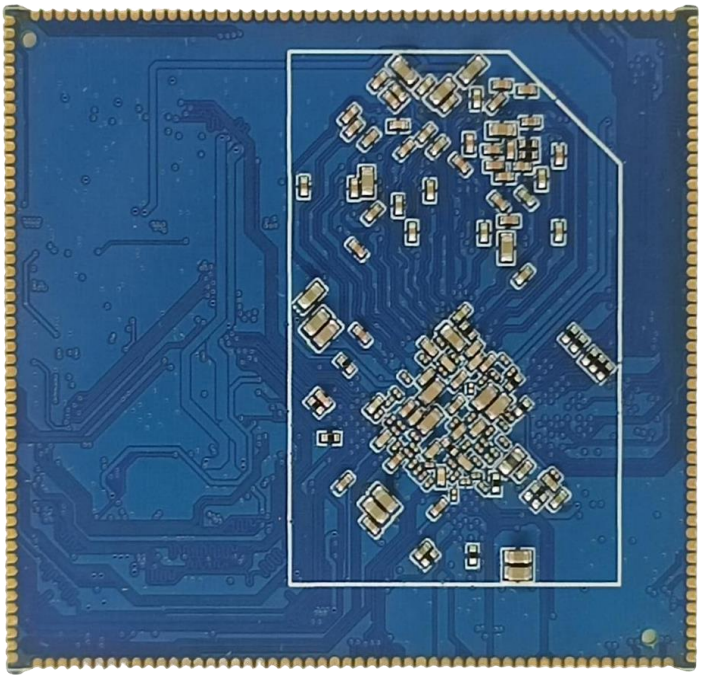
The Rockchip RK3568 series processor is a general purpose processor introduced by Rockchip, integrating Cortex-M real-time hard core, It supports 2 Gigabit Ethernet, 10 UART ports, 3 CAN-FD ports, 4 SPI ports, 6 IIC ports, HD display interface, camera interface, 3D,H.264 video hardware codec, USB interface, multi-channel serial port, PWM, ADC. It is one of the most comprehensive MPU interfaces on the market. And a long life cycle and domestic chip let you choose after no worries.



1.2 Appearance Diagram



Front drawing of the core board



Drawing of the back of the core board

Chapter 2 Hardware Parameters

2.1 Core Board Configuration Resources

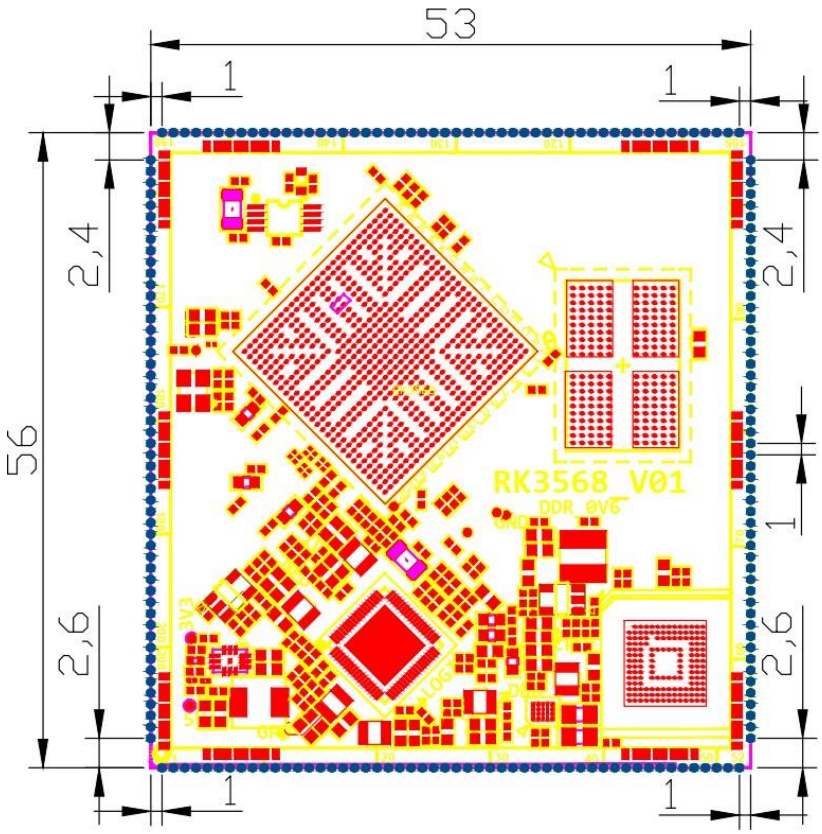
Projects	Content
CPU	Rockchip RK3568/RK3568J
Architecture	RK3568 quad core Cortex-A55@2.0GHz RK3568J quad-core Cortex-A55@1.8GHz
Memory	1GB/2GB/4GB DDR4 (default 1GB)
Flash	4GB/8GB/16GB/32GB eMMC Flash (default 8GB)
Operating Temperature	Industrial grade range: -40℃~+85℃ Commercial grade range: 0℃~+80℃
Relative Humidity	10% to 90% (no condensation)
Operating Voltage	5V voltage power supply
2D/3D	Support
GPU	Mali-G52-2EE OpenGL ES 1.1, 2.0, 3.2, Vulkan 1.0,1.1, OpenCL 2.0
NPU	1TOPS, supports mixed INT8/INT16/FP16/BFP16 operation
Operating System	Linux 5.10
MIPI DSI Display Interface	Output resolution up to 1920x1080@60Hz
LVDS Display Interface	Single channel 8 bit output, resolution up to 1280x800
HDMI Display Port	Supports maximum resolution up to 1080p@120Hz or 4096x2304@60Hz
EDP Display Interface	eDP 1.3 is supported with resolution up to 2560x1600@60Hz
Audio	1-way 8ch I2S/TDM, 2-way 2ch I2S, 1-way 8ch PDM

I2C	5-way I2C, supports 7bits and 10bits address mode, up to 1 Mbit/s rate
SPI	4-way SPI with speeds up to 50MHz
CAN	3-way CAN2.0B
USB2.0	2-way USB HOST controller, high-speed USB device (480Mbps).
USB3.0	1-way USB3.0 HOST controller, 1-way USB3.0 OTG controller.
SDIO	SDIO 3.0, data throughput up to 104MB/S
Ethernet	2 gigabit network ports, support 10/100/1000Mbps
MIPI-CSI	1-way 4 Lanes MIPI-CSI
UART	10-way UART with baud rate up to a maximum rate of 4Mbps
EINT/GPIO	More than 20 ways
PWM Timers	32bits timer/counter

2.2 Working Environment

Sequence	Environment	Minimum	Typical	Maximum
1	Power supply	4.5 V	5V	5.5 V
2	Power consumption at work	/	/	800mA
3	Operating temperature (industrial grade)	-40°C	/	+85°C
4	Operating temperature (commercial grade)	0°C	/	+80°C
5	Humidity range (no condensation)	10%RH	/	90%RH

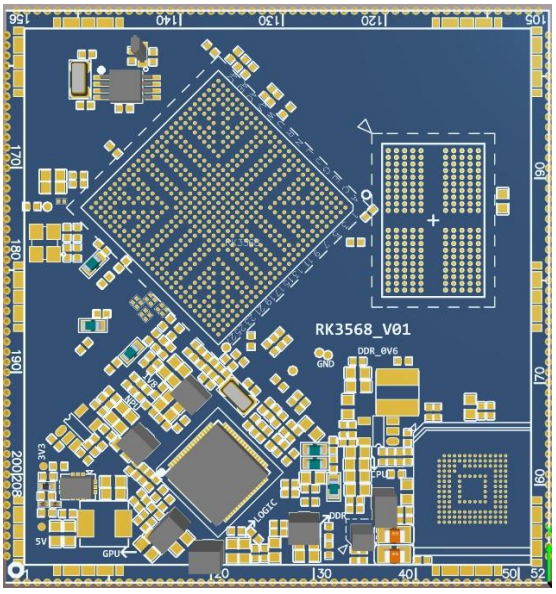
2.3 Structural Dimensions



Items	Content
Core board size	56 mm * 53 mm * 2.85 mm
Interface mode	1.0mm spacing stamp hole (208pin)

Chapter 3 Pin Definitions

3.1 Pin location



3.2 Pin Definition

Pin Num	Pin Smbol	Pin Function Introduction	MPU foot
A1	GND	Ground GND	—
A2	VCC5V0_SYS	System 5V	—
A3	VCC5V0_SYS	System 5V	—
A4	GND	System 5V	—
A5	SDMMC0_DET_L	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	Y22
A6	SDMMC0_D3	SDMMC0_D3/ARMJTAG_TMS/UART5_RTSn_M0/GPIO2_A0_u	J23
A7	SDMMC0_D2	SDMMC0_D2/ARMJTAG_TCK/UART5_CTSn_M0/GPIO1_D7_u	H26
A8	SDMMC0_D1	SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1/GPIO1_D6_u	J24

A9	SDMMC0_D0	SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1/GPIO1_D5_u	J25
A10	SDMMC0_CMD	SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1/GPIO2_A1_u	H27
A11	SDMMC0_CLK	SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1/GPIO2_A2_d	H28
A12	EXT_EN	PMU Enable	—
A13	GPIO0_D4_d	GPIO0_D4_d	AB23
A14	GPIO0_C3_d	PWM4/VOP_PWM_M0/PCIE30X1_PERSTn_M0/MCU_JTAG_TRSTn/GPIO0_C3_d	AE23
A15	SARADC_VIN0_KEY/RECOVERY	SARADC_VIN0	B27
A16	SARADC_VIN1_HW_ID	SARADC_VIN1	C26
A17	RK809_PWRON	RK809 PMIC Power On	—
A18	HPR_OUT	RK809 CODEC Headphone Right Out	—
A19	HPL_OUT	RK809 CODEC Headphone Left Out	—
A20	SPKP_OUT	RK809 CODEC SPK+ Out	—
A21	SPKN_OUT	RK809 CODEC SPK- Out	—
A22	MIC1_INP	RK809 CODEC MIC+ In	—
A23	MIC1_INN	RK809 CODEC MIC- In	—
A24	GND	Ground GND	—
A25	GMAC0_RXCLK	SDMMC1_D2/GMAC0_RXCLK/UART7_RX_M0/GPIO2_A5_u	B28
A26	GMAC0_RXD0	GMAC0_RXD0/UART1_CTSn_M0/SPI1_	F27

		MISO_M0/GPIO2_B6_u	
A27	GMAC0_RXD1	I2S2_SCLK_RX_M0/GMAC0_RXD1/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO2_B7_d	H25
A28	GMAC0_RXD2	SDMMC1_D0/GMAC0_RXD2/UART6_RX_M0/GPIO2_A3_u	E27
A29	GMAC0_RXD3	SDMMC1_D1/GMAC0_RXD3/UART6_TX_M0/GPIO2_A4_u	E28
A30	GMAC0_RXDV_CRS	I2S2_LRCK_RX_M0/GMAC0_RXDV_CRS/UART6_CTSn_M0/SPI1_CS0_M0/GPIO2_C0_d	F24
A31	GMAC0_TXEN	GMAC0_TXEN/UART1_RTSn_M0/SPI1_CLK_M0/GPIO2_B5_u	G28
A32	GMAC0_TXD0	GMAC0_TXD0/UART1_RX_M0/GPIO2_B3_u	F28
A33	GMAC0_TXD1	GMAC0_TXD1/UART1_TX_M0/GPIO2_B4_u	G27
A34	GMAC0_TXD2	SDMMC1_D3/GMAC0_TXD2/UART7_TX_M0/GPIO2_A6_u	C27
A35	GMAC0_TXD3	SDMMC1_CMD/GMAC0_TXD3/UART9_RX_M0/GPIO2_A7_u	C28
A36	GMAC0_TXCLK	SDMMC1_CLK/GMAC0_TXCLK/UART9_TX_M0/GPIO2_B0_d	D27
A37	UART8_RX_M0	CLK32K_OUT1/UART8_RX_M0/SPI1_CS1_M0/GPIO2_C6_d	E26
A38	UART8_TX_M0	I2S2_SDI_M0/GMAC0_RXER/UART8_TX_M0/SPI2_CS1_M0/GPIO2_C5_d	F26
A39	UART8_RTSN_M0	SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/CAN2_RX_M1/GPIO2_B1_d	D26
A40	UART8_CTSN_M0	SDMMC1_DET/I2C4_SCL_M1/UART8_	E25

		CTSn_M0/CAN2_TX_M1/GPIO2_B2_u	
A41	GMAC0_MDC	I2S2_LRCK_TX_M0/GMAC0_MDC/UART9_RTSn_M0/SPI2_MOSI_M0/GPIO2_C3_d	H24
A42	GMAC0_MCLKINOUT	I2S2_SCLK_TX_M0/GMAC0_MCLKINOUT/UART7_CTSn_M0/SPI2_MISO_M0/GPIO2_C2_d	F25
A43	GMAC0_MDIO	I2S2_SDO_M0/GMAC0_MDIO/UART9_CTSn_M0/SPI2_CS0_M0/GPIO2_C4_d	H23
A44	ETH0_REFCLKO_25M	I2S2_MCLK_M0/ETH0_REFCLKO_25M/UART7_RTSn_M0/SPI2_CLK_M0/GPIO2_C1_d	G23
A45	GND	Ground GND	—
A46	SARADC_VIN2_HP_HOOK	SARADC_VIN2	D24
A47	SARADC_VIN3_BOM_ID	SARADC_VIN3	E23
A48	GPIO2_D0	LCDC_D0/VOP_BT656_D0_M0/SPI0_MISO_M1/PCIE20_CLKREQn_M1/I2S1_MCLK_M2/GPIO2_D0_d	AG6
A49	GPIO2_D1	LCDC_D1/VOP_BT656_D1_M0/SPI0_MOSI_M1/PCIE20_WAKEn_M1/I2S1_SCLK_TX_M2/GPIO2_D1_d	AD7
A50	GPIO2_D2	LCDC_D2/VOP_BT656_D2_M0/SPI0_CS0_M1/PCIE30X1_CLKREQn_M1/I2S1_LRCK_TX_M2/GPIO2_D2_d	AC8
A51	GPIO2_D3	LCDC_D3/VOP_BT656_D3_M0/SPI0_CLK_M1/PCIE30X1_WAKEn_M1/I2S1_SDI0_M2/GPIO2_D3_d	AC7

A52	GPIO1_A4	I2S1_SCLK_RX_M0/UART4_RX_M0/PDM_CLK1_M0/SPDIF_TX_M0/GPIO1_A4_d	F18
A53	GPIO0_A5	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	AF25
A54	GPIO0_C1	PWM2_M0/NPUAVS/UART0_TX/MCU_JTAG_TDI/GPIO0_C1_d	AF23
A55	GPIO4_C6	PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	AE8
A56	GPIO4_C5	PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	AD8
A57	GPIO4_C4	EDP_HPDIN_M0/SPDIF_TX_M2/SATA2_ACT_LED/PCIE30X2_PERSTn_M2/I2S3_LRCK_M1/GPIO4_C4_d	AH7
A58	GPIO4_C3	PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	AA11
A59	GPIO4_C2	PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	AF8
A60	GPIO0_D5	GPIO0_D5_d	AD25
A61	GPIO0_D6	GPIO0_D6_d	AC24
A62	GPIO3_D5	PCIE30_REFCLKN_IN	AA25
A63	GPIO3_D4	CIF_D6/EBC_SDDO6/SDMMC2_DET_M0/I2S1_SDI2_M1/VOP_BT656_D6_M1/GPIO3_D4_d	AA1
A64	GPIO3_D3	CIF_D5/EBC_SDDO5/SDMMC2_CLK_M	AC1

		0/I2S1_SDI1_M1/VOP_BT656_D5_M1/GPIO3_D3_d	
A65	GPIO3_D2	CIF_D4/EBC_SDDO4/SDMMC2_CMD_M0/I2S1_SDI0_M1/VOP_BT656_D4_M1/GPIO3_D2_d	Y7
A66	GPIO3_D1	CIF_D3/EBC_SDDO3/SDMMC2_D3_M0/I2S1_SDO0_M1/VOP_BT656_D3_M1/GPIO3_D1_d	AB1
A67	GPIO3_D0	CIF_D2/EBC_SDDO2/SDMMC2_D2_M0/I2S1_LRCK_TX_M1/VOP_BT656_D2_M1/GPIO3_D0_d	AB5
A68	GND	Ground GND	—
A69	GPIO3_C7	CIF_D1/EBC_SDDO1/SDMMC2_D1_M0/I2S1_SCLK_TX_M1/VOP_BT656_D1_M1/GPIO3_C7_d	AA6
A70	GPIO3_C6	CIF_D0/EBC_SDDO0/SDMMC2_D0_M0/I2S1_MCLK_M1/VOP_BT656_D0_M1/GPIO3_C6_d	AC5
A71	GPIO3_C4	PWM14_M0/VOP_PWM_M1/GMAC1_MDC_M0/UART7_TX_M1/PDM_CLK1_M2/GPIO3_C4_d	AC3
A72	GPIO3_C3	LCDC_DEN/VOP_BT1120_D15/SPI1_CLK_M1/UART5_RX_M1/I2S1_SCLK_RX_M2/GPIO3_C3_d	AC4
A73	GPIO3_C2	LCDC_VSYNC/VOP_BT1120_D14/SPI1_MISO_M1/UART5_TX_M1/I2S1_SDO3_M2/GPIO3_C2_d	AA7
A74	GPIO3_C1	LCDC_HSYNC/VOP_BT1120_D13/SPI1_MOSI_M1/PCIE20_PERSTn_M1/I2S1_SDO2_M2/GPIO3_C1_d	AD1

A75	GPIO3_A1	LCDC_D8/VOP_BT1120_D0/SPI1_CS0_M1/PCIE30X1_PERSTn_M1/SDMMC2_D0_M1/GPIO3_A1_d	AB8
A76	GPIO3_A2	LCDC_D9/VOP_BT1120_D1/GMAC1_TXD2_M0/I2S3_MCLK_M0/SDMMC2_D1_M1/GPIO3_A2_d	AE5
A77	GPIO3_A0	LCDC_CLK/VOP_BT656_CLK_M0/SPI2_CLK_M1/UART8_RX_M1/I2S1_SDO1_M2/GPIO3_A0_d	AH4
A78	GPIO3_B6	LCDC_D21/VOP_BT1120_D12/GMAC1_TXD1_M0/I2C3_SDA_M1/PWM11_IR_M0/GPIO3_B6_d	AE3
A79	GPIO3_B5	LCDC_D20/VOP_BT1120_D11/GMAC1_TXD0_M0/I2C3_SCL_M1/PWM10_M0/GPIO3_B5_d	AE2
A80	UART4_TX_M1	LCDC_D17/VOP_BT1120_D8/GMAC1_RXD1_M0/UART4_TX_M1/PWM9_M0/GPIO3_B2_d	AF2
A81	UART4_RX_M1	LCDC_D16/VOP_BT1120_D7/GMAC1_RXD0_M0/UART4_RX_M1/PWM8_M0/GPIO3_B1_d	AG1
A82	I2S3_SDI_M0	LCDC_D13/VOP_BT1120_CLK/GMAC1_TXCLK_M0/I2S3_SDI_M0/SDMMC2_CLK_M1/GPIO3_A6_d	AG3
A83	I2S3_SDO_M0	LCDC_D12/VOP_BT1120_D4/GMAC1_RXD3_M0/I2S3_SDO_M0/SDMMC2_CMD_M1/GPIO3_A5_d	AH3
A84	I2S3_LRCK_M0	LCDC_D11/VOP_BT1120_D3/GMAC1_RXD2_M0/I2S3_LRCK_M0/SDMMC2_D3_M1/GPIO3_A4_d	AF4
A85	I2S3_SCLK_M0	LCDC_D10/VOP_BT1120_D2/GMAC1_T	AG4

		XD3_M0/I2S3_SCLK_M0/SDMMC2_D2_M1/GPIO3_A3_d	
A86	GPIO4_C0	CIF_CLKOUT/EBC_GDCLK/PWM11_IR_M1/GPIO4_C0_d	U3
A87	GPIO4_D2	GPIO4_D2_d	AB9
A88	GND	Ground GND	—
A89	I2C2_SCL_M1	I2C2_SCL_M1/EBC_SDSHR/CAN2_TX_M0/I2S1_SDO3_M1/GPIO4_B5_d	V5
A90	I2C2_SDA_M1	I2C2_SDA_M1/EBC_GDSP/CAN2_RX_M0/ISP_FLASH_TRIGIN/VOP_BT656_CLK_M1/GPIO4_B4_d	V6
A91	GPIO4_B2	I2C4_SDA_M0/EBC_VCOM/GMAC1_RXER_M1/SPI3_MOSI_M0/I2S2_SDI_M1/GPIO4_B2_d	V4
A92	GPIO0_C5	PWM6/SPI0_MISO_M0/PCIE30X2_WAKEn_M0/GPIO0_C5_d	AC21
A93	GPIO0_C4	PWM5/SPI0_CS1_M0/UART0_RTSn/GPIO0_C4_d	AD21
A94	GPIO0_C2	PWM3_IR/EDP_HPDIN_M1/PCIE30X1_WAKEn_M0/MCU_JTAG_TMS/GPIO0_C2_d	AG23
A95	GPIO0_C7	HDMITX_CEC_M1/PWM0_M1/UART0_CTSn/GPIO0_C7_d	AH25
A96	GMAC1_MCLKINOUT	CIF_CLKIN/EBC_SDCLK/GMAC1_MCLKINOUT_M1/UART1_CTSn_M1/I2S2_SCLK_RX_M1/GPIO4_C1_d	U2
A97	GMAC1_MDIO	CIF_VSYNC/EBC_SDOE/GMAC1_MDIO_M1/I2S2_SCLK_TX_M1/GPIO4_B7_d	U4
A98	GMAC1_MDC	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1/UART1_RTSn_M1/I2S2_MCLK_M1/	U5

		GPIO4_B6_d	
A99	ETH1_REFCLKO_25M	I2C4_SCL_M0/EBC_GDOE/ETH1_REFCLKO_25M_M1/SPI3_CLK_M0/I2S2_SDO_M1/GPIO4_B3_d	V1
A100	GMAC1_RXCLK	CIF_D13/EBC_SDDO13/GMAC1_RXCLK_M1/UART7_RX_M2/PDM_SDI3_M1/GPIO4_A3_d	Y3
A101	GMAC1_RXD3	CIF_D12/EBC_SDDO12/GMAC1_RXD3_M1/UART7_TX_M2/PDM_SDI2_M1/GPIO4_A2_d	Y4
A102	GMAC1_RXD2	CIF_D11/EBC_SDDO11/GMAC1_RXD2_M1/PDM_SDI1_M1/GPIO4_A1_d	AA2
A103	GMAC1_RXD1	CAM_CLKOUT1/EBC_SDCE2/GMAC1_RXD1_M1/SPI3_MISO_M0/I2S1_SDO1_M1/GPIO4_B0_d	V7
A104	GMAC1_RXD0	CAM_CLKOUT0/EBC_SDCE1/GMAC1_RXD0_M1/SPI3_CS1_M0/I2S1_LRCK_RX_M1/GPIO4_A7_d	W1
A105	GMAC1_RXDV_CRS	ISP_PRELIGHT_TRIG/EBC_SDCE3/GMAC1_RXDV_CRS_M1/I2S1_SDO2_M1/GPIO4_B1_d	V2
A106	GMAC1_TXD0	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1/UART9_TX_M2/I2S2_LRCK_TX_M1/GPIO4_A4_d	Y2
A107	GMAC1_TXD1	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1/UART9_RX_M2/I2S2_LRCK_RX_M1/GPIO4_A5_d	Y1
A108	GMAC1_TXD2	CIF_D8/EBC_SDDO8/GMAC1_TXD2_M1/UART1_TX_M1/PDM_CLK0_M1/GPIO3_D6_d	Y6
A109	GMAC1_TXD3	CIF_D9/EBC_SDDO9/GMAC1_TXD3_M	Y5

		1/UART1_RX_M1/PDM_SDI0_M1/GPIO3_D7_d	
A110	GMAC1_TXEN	ISP_FLASHTRIGOUT/EBC_SDCE0/GMAC1_TXEN_M1/SPI3_CS0_M0/I2S1_SCLK_RX_M1/GPIO4_A6_d	W2
A111	GMAC1_TXCLK	CIF_D10/EBC_SDDO10/GMAC1_TXCLK_M1/PDM_CLK1_M1/GPIO4_A0_d	AA3
A112	GPIO3_B0	LCDC_D15/VOP_BT1120_D6/ETH1_REFCLKO_25M_M0/SDMMC2_PWREN_M1/GPIO3_B0_d	AG2
A113	GPIO0_B7	PWM0_M0/CPUAVS/GPIO0_B7_d	AH26
A114	GPIO3_C5	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	AC2
A115	GPIO3_C0	LCDC_D23/PWM13_M0/GMAC1_MCLKINOUT_M0/UART3_RX_M1/PDM_SDI3_M2/GPIO3_C0_d	AD2
A116	GPIO3_B7	LCDC_D22/PWM12_M0/GMAC1_TXEN_M0/UART3_TX_M1/PDM_SDI2_M2/GPIO3_B7_d	AD4
A117	I2C5_SDA_M0	LCDC_D19/VOP_BT1120_D10/GMAC1_RXER_M0/I2C5_SDA_M0/PDM_SDI1_M2/GPIO3_B4_d	AE1
A118	I2C5_SCL_M0	LCDC_D18/VOP_BT1120_D9/GMAC1_RXDV_CRS_M0/I2C5_SCL_M0/PDM_SDI0_M2/GPIO3_B3_d	AF1
A119	GND	Ground GND	—
A120	USB2_HOST2_DM	USB2_HOST2_DM	R1
A121	USB2_HOST2_DP	USB2_HOST2_DP	R2

A122	USB2_HOST3_DM	USB2_HOST3_DM	T1
A123	USB2_HOST3_DP	USB2_HOST3_DP	T2
A124	GPIO2_D4	LCDC_D4/VOP_BT656_D4_M0/SPI2_CS1_M1/PCIE30X2_CLKREQn_M1/I2S1_SDI1_M2/GPIO2_D4_d	AF5
A125	GPIO2_D5	LCDC_D5/VOP_BT656_D5_M0/SPI2_CS0_M1/PCIE30X2_WAKEn_M1/I2S1_SDI2_M2/GPIO2_D5_d	AF6
A126	GPIO2_D6	LCDC_D6/VOP_BT656_D6_M0/SPI2_MOSI_M1/PCIE30X2_PERSTn_M1/I2S1_SDI3_M2/GPIO2_D6_d	AD6
A127	GPIO2_D7	LCDC_D7/VOP_BT656_D7_M0/SPI2_MISO_M1/UART8_TX_M1/I2S1_SDO0_M2/GPIO2_D7_d	AH5
A128	GPIO3_A7	LCDC_D14/VOP_BT1120_D5/GMAC1_RXCLK_M0/SDMMC2_DET_M1/GPIO3_A7_d	AH2
A129	HDMITX_SCL	HDMITX_SCL/I2C5_SCL_M1/GPIO4_C7_u	AG8
A130	HDMITX_SDA	HDMITX_SDA/I2C5_SDA_M1/GPIO4_D0_u	AG7
A131	HDMITX_CEC_M0	HDMITX_CEC_M0/SPI3_CS1_M1/GPIO4_D1_u	AH6
A132	HDMITX_HPDIN	HDMI_TX_HPDIN	AB18
A133	GND	Ground GND	—
A134	MIPI_CSI_RX_D3N	MIPI_CSI_RX_D3N	AE9
A135	MIPI_CSI_RX_D3P	MIPI_CSI_RX_D3P	AD9

A136	MIPI_CSI_RX_D2N	MIPI_CSI_RX_D2N	AD11
A137	MIPI_CSI_RX_D2P	MIPI_CSI_RX_D2P	AE11
A138	MIPI_CSI_RX_CLK1N	MIPI_CSI_RX_CLK1N	AH9
A139	MIPI_CSI_RX_CLK1P	MIPI_CSI_RX_CLK1P	AG9
A140	MIPI_CSI_RX_CLK0N	MIPI_CSI_RX_CLK0N	AH10
A141	MIPI_CSI_RX_CLK0P	MIPI_CSI_RX_CLK0P	AG10
A142	MIPI_CSI_RX_D1N	MIPI_CSI_RX_D1N	AH11
A143	MIPI_CSI_RX_D1P	MIPI_CSI_RX_D1P	AG11
A144	MIPI_CSI_RX_D0N	MIPI_CSI_RX_D0N	AH12
A145	MIPI_CSI_RX_D0P	MIPI_CSI_RX_D0P	AG12
A146	GND	Ground GND	—
A147	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	AH13
A148	MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	AG13
A149	MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	AH14
A150	MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	AG14
A151	MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP	MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	AH15
A152	MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	AG15
A153	MIPI_DSI_TX0_D1P/LV	MIPI_DSI_TX0_D1P/LVDS_TX0_D1P	AH16

	DS_TX0_D1P		
A154	MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	AG16
A155	MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	AH17
A156	MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	AG17
A157	HDMI_TXCLKN	HDMI_TX_CLKN	AG19
A158	HDMI_TXCLKP	HDMI_TX_CLKP	AH19
A159	HDMI_TX0N	HDMI_TX_D0N	AH20
A160	HDMI_TX0P	HDMI_TX_D0P	AG20
A161	HDMI_TX1N	HDMI_TX_D1N	AH21
A162	HDMI_TX1P	HDMI_TX_D1P	AG21
A163	HDMI_TX2N	HDMI_TX_D2N	AH22
A164	HDMI_TX2P	HDMI_TX_D2P	AG22
A165	GND	Ground GND	—
A166	GPIO0_C0	PWM1_M0/GPUAVS/UART0_RX/GPIO0_C0_d	AD22
A167	PWM7_IR	PWM7_IR/SPI0_CS0_M0/PCIE30X2_PERSTn_M0/GPIO0_C6_d	AD20
A168	UART2_RX_M0_DEBUG	UART2_RX_M0/GPIO0_D0_u	AC20
A169	UART2_TX_M0_DEBUG	UART2_TX_M0/GPIO0_D1_u	AH24
A170	I2C1_SCL_TP	I2C1_SCL/CAN0_TX_M0/PCIE30X1_BUTTONRSTn/MCU_JTAG_TDO/GPIO0_B	AG24

		3_u	
A171	I2C1_SDA_TP	I2C1_SDA/CAN0_RX_M0/PCIE20_BUTTONRSTn/MCU_JTAG_TCK/GPIO0_B4_u	AB20
A172	TP_INT_L_GPIO0_B5	I2C2_SCL_M0/SPI0_CLK_M0/PCIE20_WAKEn_M0/PWM1_M1/GPIO0_B5_u	AC22
A173	TP_RST_L_GPIO0_B6	I2C2_SDA_M0/SPI0_MOSI_M0/PCIE20_PERSTn_M0/PWM2_M1/GPIO0_B6_u	AA20
A174	RK809_32KOUT_WIFI	RK809 WIFI的32K输出	—
A175	RESETn	RK809 Reset	—
A176	GPIO0_A6	GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	AE24
A177	GND	Ground GND	—
A178	PCIE20_REFCLKN	PCIE20_REFCLKN	V25
A179	PCIE20_REFCLKP	PCIE20_REFCLKP	V24
A180	PCIE20_RXN	PCIE20_RXN/SATA2_RXN/QSGMII_RXN_M1	Y28
A181	PCIE20_RXP	PCIE20_RXP/SATA2_RXP/QSGMII_RXP_M1	Y27
A182	PCIE20_TXN	PCIE20_TXN/SATA2_TXN/QSGMII_TXN_M1	W28
A183	PCIE20_TXP	PCIE20_TXP/SATA2_TXP/QSGMII_TXP_M1	W27
A184	GND	Ground GND	—
A185	USB3_HOST1_SSTXP	USB3_HOST1_SSTXP/SATA1_TXP/QSGMII_TXP_M0	V28
A186	USB3_HOST1_SSTXN	USB3_HOST1_SSTXN/SATA1_TXN/QSGMII_TXN_M0	V27

A187	USB3_HOST1_SSRXP	USB3_HOST1_SSRXP/SATA1_RXP/QSGMII_RXP_M0	U28
A188	USB3_HOST1_SSRXN	USB3_HOST1_SSRXN/SATA1_RXN/QSGMII_RXN_M0	U27
A189	USB3_OTG0_SSTXP	USB3_OTG0_SSTXP/SATA0_TXP	T28
A190	USB3_OTG0_SSTXN	USB3_OTG0_SSTXN/SATA0_TXN	T27
A191	USB3_OTG0_SSRXP	USB3_OTG0_SSRXP/SATA0_RXP	R28
A192	USB3_OTG0_SSRXN	USB3_OTG0_SSRXN/SATA0_RXN	R27
A193	USB3_OTG0_DM	USB3_OTG0_DM	P28
A194	USB3_OTG0_DP	USB3_OTG0_DP	P27
A195	USB3_HOST1_DM	USB3_HOST1_DM	P25
A196	USB3_HOST1_DP	USB3_HOST1_DP	P24
A197	USB3_OTG0_VBUSDET	USB3_OTG0_VBUSDET	M24
A198	USB3_OTG0_ID	USB3_OTG0_ID	L23
A199	EDP_TX_D3N	EDP_TX_D3N	N27
A200	EDP_TX_D3P	EDP_TX_D3P	M28
A201	EDP_TX_D2N	EDP_TX_D2N	M27
A202	EDP_TX_D2P	EDP_TX_D2P	L28
A203	EDP_TX_AUXN	EDP_TX_AUXN	M25
A204	EDP_TX_AUXP	EDP_TX_AUXP	L25
A205	EDP_TX_D1N	EDP_TX_D1N	L27
A206	EDP_TX_D1P	EDP_TX_D1P	K28

A207	EDP_TX_D0N	EDP_TX_D0N	K27
A208	EDP_TX_D0P	EDP_TX_D0P	J28

Chapter 4 Core Board Instructions

4.1 Hardware Design

4.1.1 DDR4 Memory

The system uses 16bit DDR4 SDRAM connected to the DDR interface of RK3568S, which is compatible with 512MB/1GB/2GB DDR4 and can work at a maximum data frequency of 1600Mbps.

4.1.2 Flash Storage

The RK3568S storage scheme has eMMC storage.

eMMC is a solution of embedded Flash chip with standardized interface, which simplifies the interface design and solves the problem of driver compatibility caused by the different standards between Flash manufacturers. When using eMMC, it is connected to the MMC0 port of G2L, 8-bit MMC data cable width, capacity of 4GB/8GB/16GB/32GB.

4.1.3 Power Supply

RK3568S adopts power management scheme, PMIC is selected as RK809, power on 5V operation.

4.1.4 Ethernet

RK3568S supports two gigabit network ports, the two network ports are provided in the form of RGMII, connected to the external interface of the core board, users can easily use the network port directly, or for other I/O ports.

4.2 Default Function of Core Board Pin

4.2.1 HDMI

RK3568S series core board with 1 HDMI channel.

Pin Number	Signal	Description
A157	HDMI_TXCLKN	HDMI Clock -
A158	HDMI_TXCLKP	HDMI Clock+
A159	HDMI_TX0N	HDMI Data0 -

A160	HDMI_TX0P	HDMI Data0+
A161	HDMI_TX1N	HDMI Data1 -
A162	HDMI_TX1P	HDMI Data1 +
A163	HDMI_TX2N	HDMI Data2 -
A164	HDMI_TX2P	HDMI Data2 +
A165	GND	Ground

4.2.2 Two-way Gigabit Ethernet

Pin Number	Signal	Description
A96	GMAC1_MCLKINOUT_M1	GMAC1's 125MHz Clock M1
A97	GMAC1_MDIO_M1	GMAC1 Data Management M1
A98	GMAC1_MDC_M1	GMAC1 Clock Management M1
A99	ETH1_REFCLKO_25M_M1	ETH1 5MHz Reference Clock M1
A100	GMAC1_RXCLK_M1	GMAC1 Receives Clock M1
A101	GMAC1_RXD3_M1	GMAC1 Receives Data3 M1
A102	GMAC1_RXD2_M1	GMAC1 Receives Data 2 M1
A103	GMAC1_RXD1_M1	GMAC1 Receives Data 1 M1
A104	GMAC1_RXD0_M1	GMAC1 Receives Data 0 M1
A105	GMAC1_RXDV_CRS_M1	GMAC1 Receive Data Control M1
A106	GMAC1_TXD0_M1	GMAC1 Send Data 0 M1
A107	GMAC1_TXD1_M1	GMAC1 Send Data 1 M1
A108	GMAC1_TXD2_M1	GMAC1 Send Data 2 M1

A109	GMAC1_TXD3_M1	GMAC1 Send Data 3 M1
A110	GMAC1_TXEN_M1	GMAC1 Send Enable M1
A111	GMAC1_TXCLK_M1	GMAC1 Send Clock M1
A112	ETH1_REFCLKO_25M_M0	ETH1 25MHz Reference Clock M0
A114	GMAC1_MDIO_M0	GMAC1 Serial Data Management M0
A115	GMAC1_MCLKINOUT_M0	GMAC1 125MHz Clock M0
A116	GMAC1_TXEN_M0	GMAC1 Send Enable M0
A117	GMAC1_RXER_M0	GMAC1 Receives Data Error M0
A118	GMAC1_RXDV_CRS_M0	GMAC1 Receives Data Control M0
A119	GND	Ground GND

Pin Number	Signal	Description
A25	GMAC0_RXCLK	GMAC0 Receives Clock
A26	GMAC0_RXD0	GMAC0 Receives Data 0
A27	GMAC0_RXD1	GMAC0 Receives Data 1
A28	GMAC0_RXD2	GMAC0 Receives Data 2
A29	GMAC0_RXD3	GMAC0 Receives Data 3
A30	GMAC0_RXDV_CRS	GMAC0 Receives Data Control
A31	GMAC0_TXEN	GMAC0 Send Enable
A32	GMAC0_TXD0	GMAC0 Sends Data 0
A33	GMAC0_TXD1	GMAC0 Sends Data 1
A34	GMAC0_TXD2	GMAC0 Send Data 2

A35	GMAC0_TXD3	GMAC0 Send Data 3
A36	GMAC0_TXCLK	GMAC0 Send Clock
A38	GMAC0_RXER	GMAC0 Received Data Error
A41	GMAC0_MDC	GMAC0 Serial Clock Management
A42	GMAC0_MCLKINOUT	GMAC0 125MHz Synchronous Clock
A43	GMAC0_MDIO	GMAC0 Serial Data management
A44	ETH0_REFCLKO_25M	ETH0 25MHz Reference Clock
A45	GND	Ground GND

4.2.3 MIPI Interface and LVDS Interface

Pin Number	Signal	Description
A133	GND	Ground
A134	MIPI_CSI_RX_D3N	MIPI1 Data 3-
A135	MIPI_CSI_RX_D3P	MIPI1 Data 3+
A136	MIPI_CSI_RX_D2N	MIPI1 Data 2-
A137	MIPI_CSI_RX_D2P	MIPI1 Data 2+
A138	MIPI_CSI_RX_CLK1N	MIPI1 Clock 1-
A139	MIPI_CSI_RX_CLK1P	MIPI1 Clock 1+
A140	MIPI_CSI_RX_CLK0N	MIPI1 Clock 0-
A141	MIPI_CSI_RX_CLK0P	MIPI1 Clock 0+
A142	MIPI_CSI_RX_D1N	MIPI1 Data 1-
A143	MIPI_CSI_RX_D1P	MIPI1 Data 1+
A144	MIPI_CSI_RX_D0N	MIPI1 Data 0-
A145	MIPI_CSI_RX_D0P	MIPI1 Data 0+

A146	GND	Ground GND
A147	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	MIPI0 Data 3+/LVDS Data 3+
A148	MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	MIPI0 Data 3-/LVDS Data 3-
A149	MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	MIPI0 Data 2+/LVDS Data 2+
A150	MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	MIPI0 Data 2-/LVDS Data 2-
A151	MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP	MIPI0 Clock +/LVDS Clock +
A152	MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	MIPI0 Clock -/LVDS Clock -
A153	MIPI_DSI_TX0_D1P/LVDS_TX0_D1P	MIPI0 Data 1-/LVDS Data 1+
A154	MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	MIPI0 Data 1+/LVDS Data 1-
A155	MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	MIPI0 Data 0-/LVDS Data 0+
A156	MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	MIPI0 Data 0+/LVDS Data 0-

Chapter 5 Software Parameters

Core board software parameters:

Linux kernel	Linux5.10, Android12	
Filesystems	Yocto	
Support Driver	DDR4	eMMC Flash
	MMC/SD	Audio
	LCD MIPI/HDMI out	Ethernet
	Usb/start	UART
	PWM	RS485
	USB 4G	I2C
	RTC	LVDS
	SDIO WIFI	MIPI CSI
	KEY	TouchScreen

Chapter 6 Order Model

Model Number	Description
WTC-RK3568S-A	RK3568S core board 1.8GHZ, 1GB DDR4, 8GB eMMC

The above model is the standard configuration, the other configuration can be customized, but there are MOQ requirements, please consult sales for details.

Chapter 7 Declaration

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